AMENDMENTS TO THE SPECIFICATION

In Paragraph 0038, please incorporate the changes as indicated:

[0038]   Figure 1 is a functional block diagram illustrating a master in communication with a slave over a bus according to one embodiment of the present invention. A master 104 communicates with a slave 108 over a bus 112. The master is coupled to a master sample cycle generator module 116 to receive a sample cycle signal over a line 124. The master sample cycle module 116 receives a copy of the master's internal clock over a line 120. A bus clock 126 [[and]] generates the sample cycle signal 124 for the master according to the two clock inputs. Similarly, a slave 108 is coupled to a slave sample cycle generator module 118 which provides the sample cycle signal 128 to it. The sample cycle block receives a copy of the slave's internal clock 132 and the bus clock 126 and generates the sample cycle signal 128 for the slave, accordingly. The sample cycle signal 128 determines when the master 104 is placing valid data on the bus that is to be latched.

In Paragraph 0044, please incorporate the changes as indicated:

[0044]   Without issuing sample pulses to prompt the slave 108 to latch the bus [[on]] 112, the slave would not know on which of its (B clock) clock cycles to latch the bus. The reason is that the slave is operating at a much higher rate of speed than the bus (A clock). Accordingly, whether the slave latches good data or bad data depends on its ability to accurately determine when the bus has valid data. Thus, the internal state machine generates a sample clock signal whenever it is time to sample, or read, the data. Thus, as may be seen in Figure 2, the state machine, after determining the ratio of clock pulses between the A clock and the B clock, is able to determine when the sample cycle signal, as shown in Figure 2, is to be generated. Furthermore, the device always drives its output bus, or writes to its outputs, in the CLKB cycle following the sample cycle pulse.

In Paragraph 0062, please incorporate the changes as indicated:

[0062]   Once bus arbiter 628 (and/or clock generation controller 632) determines a corresponding bus frequency, the bus arbiter [[636]] 628 (and the clock generation controller 632) sets the clock rate for bus 620 to the new clock rate before it generates the grant signal to master 624. At this point, the bus is granted by the arbiter 628 to master 624. Thereafter, master 624 generates its transaction at the clock speed that is established for the bus 620 and that is being generated by bus arbiter 628.

In Paragraph 0063, please incorporate the changes as indicated:

[0063]   Once second master 624 starts a transaction on bus 620, which transaction is at a frequency that is equal to that of bus 620 as specified by bus arbiter 628 (and/or clock generation controller 632), slave 616 must determine the relative difference between its internal clock frequency rate and the clock frequency rate of bus 620. The algorithm for determining the relative difference in the frequency rates, as previously described, is implemented by a state machine 648 that is formed within slave [[616]] 608. As may be seen, slave [[608]] 612 also includes a similar state machine [[652]] 652 and slave [[612]] 616 includes a similar state machine [[656]] 656. Thus, after two transient cycles, state machine 648 generates correct internal sample cycle pulses which enable slave [[616]] 608 to determine when there is valid data on bus 620 as a part of the transaction being generated by second master 624. Each of the state machines 648, 652 and 656 of slaves 616, 608, and 612, respectively, continuously monitor communications on bus 620 to determine the relative clock rate of bus 620 to their own internal clock rates.

In Paragraph 0074, please incorporate the changes as indicated:

[0074]   Figure 8 is a table that illustrates the relationship between the various determinations about the transaction and the frequency. More specifically, the transaction transactions speed table 800 of Figure 8 lists a plurality of columns 804, 808, 812, 816, and 820, and a plurality of rows 824, 828, 832, 836, and 840, that are used to identify the appropriate bus frequency or speed. For example, the column shown generally at 804 lists each of the masters to the transaction. Column 808 lists

each of the slaves of the transaction. Note that the slave of row 824 is the master of rows 832 and 840. Thus, a master can be a slave for a particular transaction.